ABSTRACT

A digital image signal is serially transferred to each of pixels through a drain signal line. The digital image signal is sampled at pixel selecting transistors, converted from a serial signal to a parallel signal, and then converted to an analog image signal by a DA converter. This DA converter includes a plurality of capacitor electrodes coupled to a pixel electrode at a weighted capacitance ratio and a clock supplying portion for supplying periodic clock signals to the plurality of the capacitor electrodes in response to the digital image signal. The analog image signal is applied to the pixel electrode. This simplifies a configuration of peripheral circuits of the pixel, and accordingly reduces the frame area of a panel and the number of wiring lines.